

WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:
 - a first fin structure comprising a dielectric material and including a first side surface and a second side surface;
 - a second fin structure comprising a single-crystal silicon material and being
 - 5 formed adjacent to the first side surface of the first fin structure;
 - a third fin structure comprising the single-crystal silicon material and being formed adjacent to the second side surface of the first fin structure;
 - a source region formed at one end of the first fin structure, the second fin structure, and the third fin structure;
 - 10 a drain region formed at an opposite end of the first fin structure, the second fin structure, and the third fin structure; and
 - at least one gate.
2. The semiconductor device of claim 1 wherein a width of the first fin structure ranges from about 200 Å to about 1000 Å.
3. The semiconductor device of claim 1 wherein the dielectric material includes one of an oxide and a nitride.
4. The semiconductor device of claim 1 wherein a width of each of the second fin structure and the third fin structure ranges from about 100 Å to about 1000 Å.
5. A method of manufacturing a semiconductor device that includes a substrate and a dielectric layer formed on the substrate, the method comprising:

- etching the dielectric layer to form a first fin structure;
 - depositing an amorphous silicon layer;
 - 5 etching the amorphous silicon layer to form a second fin structure adjacent a first side surface of the first fin structure and a third fin structure adjacent a second, opposite side surface of the first fin structure;
 - depositing a metal layer on at least upper surfaces of the second fin structure and the third fin structure;
 - 10 performing a metal-induced crystallization operation to convert the amorphous silicon in the second and third fin structures to a single-crystal silicon material;
 - forming a source region and a drain region;
 - depositing a gate material over the first, second, and third fin structures; and
 - patterning and etching the gate material to form at least one gate electrode.
6. The method of claim 5 wherein a width of the first fin structure ranges from about 200 Å to about 1000 Å.
7. The method of claim 5 wherein the dielectric layer comprises at least one of an oxide and a nitride.
8. The method of claim 5 wherein a width of each of the second fin structure and the third fin structure ranges from about 100 Å to about 1000 Å.
9. The method of claim 5 further comprising:
- forming a second dielectric layer prior to depositing the metal layer; and

planarizing the second dielectric layer to expose upper surfaces of the second fin structure and the third fin structure.

10. The method of claim 5 wherein the performing a metal-induced crystallization operation forms a metal-silicon compound at a bottom surface of each of the second fin structure and the third fin structure.

11. The method of claim 10 wherein a thickness of the metal-silicon compound ranges from about 20 Å to about 200 Å.

12. The method of claim 5 wherein the depositing a metal layer includes:
depositing a nickel layer to a thickness of about 20 Å.

13. The method of claim 5 wherein the performing includes:
annealing the second fin structure and the third fin structure at a temperature of about 500 °C to about 550 °C.

14. The method of claim 13 wherein the annealing is performed for at least two hours.

15. A semiconductor device comprising:
a first fin structure comprising a single-crystal silicon material;
a second fin structure comprising the single-crystal silicon material; and

a third fin structure located between the first fin structure and the second fin
5 structure and comprising a dielectric material, the third fin structure causing stress to be induced
in the single-crystal silicon material of the first fin structure and the second fin structure.

16. The semiconductor device of claim 15 wherein a width of each of the first fin
structure and the second fin structure ranges from about 100 Å to about 1000 Å.

17. The semiconductor device of claim 16 wherein a width of the third fin structure
ranges from about 100 Å to about 1000 Å.

18. The semiconductor device of claim 17 wherein the dielectric material comprises
at least one of an oxide and a nitride.

19. The semiconductor device of claim 15 further comprising:
a source region located at one end of the first fin structure, the second fin
structure, and the third fin structure;
a drain region located at an opposite end of the first fin structure, the second fin
5 structure, and the third fin structure; and
at least one gate.